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EXAMINER	
LEUNG, CHRISTINA Y	
ART UNIT	**PAPER NUMBER**
2613	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/657,554	Applicant(s) ARONSON ET AL.	
	Examiner Christina Y. Leung	Art Unit 2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7* is/are allowed.

6)☒ Claim(s) *8-20 and 23-38* is/are rejected.

7)☒ Claim(s) *21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-21-04; 3-22-06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 8-20 and 23-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Stewart et al. (US 2003/0210917 A1).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 8, Stewart et al. disclose an integrated circuit 110 for controlling an optoelectronic transceiver having a laser transmitter 103 and a photodiode receiver 102 (Figures 2 and 3), comprising:

memory (EEPROMs 120, 122, and 128), including one or more memory arrays for storing information related to the transceiver in predefined memory mapped locations of the memory, the stored information including digital values corresponding to current operating conditions of the optoelectronic transceiver, where the digital values include a temperature of the

optoelectronic transceiver, an internal supply voltage of the optoelectronic transceiver, a laser bias current of the laser transmitter, an output power of the laser transmitter, and a received optical power of the photodiode receive (page 3, paragraphs [0035]-[0037]);

analog to digital conversion circuitry 127 for receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic transceiver, converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one of the predefined memory mapped locations in the memory (page 3, paragraphs [0035]-[0037]);

control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory (page 3, paragraphs [0033]-[0034]);

an interface 121 for allowing a host to read from host specified locations within the memory, including the predefined memory mapped locations of the memory, so as to obtain one or more of the digital values corresponding to current operating conditions of the optoelectronic transceiver (page 3, paragraphs [0029]-[0037]); and

wherein the control circuitry includes circuitry configured to adjust one or more control signals in accordance with an adjustment value stored in the memory by the host via the interface (Stewart et al. disclose adjustment/"margining" values; page 3, paragraph [0031]).

Regarding claim 9, Stewart et al. disclose that the adjustment value corresponds to a deviation from a configured operating condition of the optoelectronic transceiver (page 3, paragraph [0031]).

Regarding claim 10, Stewart et al. disclose that the control circuitry is configured to adjust the one or more control signals by scaling the control signals (page 3, paragraph [0031]).

Regarding claim 11, Stewart et al. disclose that the control circuitry is configured to adjust the one or more control signals by an amount specified by the adjustment value (page 3, paragraph [0031]).

Regarding claim 12, Stewart et al. disclose a method of controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver (Figures 2 and 3), comprising:

in accordance with instructions received from a host device, enabling the host device to read from and write to host specified locations within a controller of the optoelectronic transceiver (using interface 121 and EEPROMs 120, 122, and 128), the host specified locations including a set of predefined memory mapped locations in which are stored digital values corresponding to current operating conditions of the optoelectronic transceiver, the stored digital values including a temperature of the optoelectronic transceiver, an internal supply voltage of the optoelectronic transceiver, a laser bias current of the laser transmitter, an output power of the laser transmitter, and a received optical power of the photodiode receiver (page 3, paragraphs [0035]-[0037]);

receiving a plurality of analog signals from the laser transmitter 103 and photodiode receiver 102, converting the received analog signals into digital values (using analog to digital converter 127), and storing the digital values in the controller (in EEPROMs 120, 122, and 128), the converted digital values including the digital values corresponding to current operating conditions of the optoelectronic transceiver (page, paragraphs [0035]-[0037]); and

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in predefined memory mapped locations within the controller (page 3, paragraphs [0033]-[0034]); and

testing operation of the device at a known deviation from a configured operating condition of the optoelectronic transceiver by adjusting one or more control signals in accordance with an adjustment value stored in the controller (Stewart et al. disclose adjustment/"margining" values; page 3, paragraph [0031]).

Regarding claim 13, Stewart et al. disclose that the adjusting includes scaling the control signals by the adjustment value (page 3, paragraph [0031]).

Regarding claim 14, Stewart et al. disclose a circuit for an optoelectronic transceiver, which includes a laser transmitter and a photodiode receiver (Figures 2 and 3), the circuit comprising:

analog to digital conversion circuitry 127 configured to convert analog signals corresponding to operating conditions of the optoelectronic transceiver into digital values (page 3, paragraphs [0035]-[0037]);

memory (EEPROMs 120, 122, and 128) configured to store the digital values in predefined memory mapped locations, where the digital values stored in the predefined memory mapped locations include: a temperature of the optoelectronic transceiver, an internal supply voltage of the optoelectronic transceiver, a laser bias current of the laser transmitter, an output power of the laser transmitter, and a received optical power of the photodiode receiver (page 3, paragraphs [0035]-[0037]); and

an interface 121 configured to enable a host to read from the predefined memory mapped locations in memory (page 3, paragraphs [0029]-[0037]).

Regarding claim 15, Stewart et al. disclose that each of the predefined memory mapped locations are associated with a unique address in the memory (Table 1 on pages 5-7 discloses unique addresses).

Regarding claim 16, Stewart et al. disclose that each of the digital values is a 16 bit number (Table 2 on pages 7 and 8 discloses "16 bit data").

Regarding claim 17, Stewart et al. disclose a temperature sensor 125 for measuring the temperature of the optoelectronic transceiver (page 3, paragraph [0034]).

Regarding claim 18, Stewart et al. disclose a supply voltage sensor 126 for measuring the supply voltage of the optoelectronic transceiver (page 3, paragraph [0037]).

Regarding claim 19, Stewart et al. disclose that the interface is also configured to enable the host to read from and write to host-specified memory mapped addresses within the memory (page 3, paragraph [0029]).

Regarding claim 20, Stewart et al. disclose comparison logic 131 configured to compare at least one of the digital values with a limit value to generate a flag value (page 3, paragraphs [0031] and [0036]; Table 3 on pages 8 and 9 also discloses flag values generated after a comparison of a digital value to a limit value).

Regarding claim 23, Stewart et al. disclose that the limit value is dependent on the temperature of the optoelectronic transceiver (pages 8 and 9, Table 3).

Regarding claim 24. Stewart et al. disclose control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in memory (page 3, paragraphs [0033]-[0034]).

Regarding claim 25, Stewart et al. disclose that the control circuitry includes operation disable circuitry configured to disable operation of at least part of the optoelectronic transceiver (page 3, paragraph [0029]; see also page 1, paragraph [0005]).

Regarding claim 26, Stewart et al. disclose that the memory further comprises one or more memory arrays for storing information related to the optoelectronic transceiver (page 4, paragraph [0041]; see also Table 1 on pages 5-7).

Regarding claims 27 and 28, Stewart et al. disclose that a portion of the memory is reserved for optional warning flags selected from a group consisting of: a temperature high warning, a temperature low warning, a high supply voltage warning, a low supply voltage warning, a high laser bias current warning, a low laser bias current warning, a high output power warning, a low output power warning, a high received optical power warning, and a low received optical power warning (Table 3 on pages 8 and 9 discloses warning flags).

Regarding claims 29 and 30, Stewart et al. disclose that a portion of the memory is reserved for optional alarm flags selected from a group consisting of: a temperature high alarm, a temperature low alarm, a high supply voltage alarm, a low supply voltage alarm, a high laser bias current alarm, a low laser bias current alarm, a high output power alarm, a low output power alarm, a high received optical power alarm, and a low received optical power alarm (Table 3 on pages 8 and 9 discloses alarm flags).

. Regarding claims 31, 32, and 33, Stewart et al. disclose that a portion of the memory is reserved for an optional indication of a state of a transmitter disable input pin, an optional indication of a state of a software disable, and a password that controls access to the memory (Table 2 on page 8 discloses a disable state indication, and Table 1 on page 7 discloses a password).

Regarding claim 34, Stewart et al. disclose a circuit for an optoelectronic transceiver (Figures 2 and 3), comprising:

analog to digital conversion circuitry 127 configured to convert analog signals corresponding to operating conditions of an optoelectronic transceiver into 16 bit digital values (page 3, paragraphs [0035]-[0037]); Table 2 on pages 7 and 8 discloses "16 bit data");

memory (EEPROMs 120, 122, and 128) configured to store the digital values in predefined memory mapped locations identified by unique addresses, where the digital values comprise: a temperature of the optoelectronic transceiver, an internal supply voltage of the optoelectronic transceiver, a laser bias current of a laser transmitter of the optoelectronic transceiver, an output power of the laser transmitter, and a received optical power of a photodiode receiver of the optoelectronic transceiver (page 3, paragraphs [0035]-[0037]); and

an interface 121 configured to enable a host having the addresses to read the digital values from the predefined memory mapped locations in memory (page 3, paragraphs [0029]-[0037]).

Regarding claim 35, Stewart et al. disclose a temperature sensor 125 for measuring the temperature of the optoelectronic transceiver (page 3, paragraph [0034]) and a supply voltage sensor 126 for measuring the supply voltage of the optoelectronic transceiver (page 3, paragraph

Regarding claim 36, Stewart et al. disclose that the interface is also configured to enable the host to read from and write to host-specified memory mapped locations within the memory (page 3, paragraph [0029]).

Regarding claim 37, Stewart et al. disclose that a portion of the memory is reserved for information selected from a group consisting of: optional warning flags, optional alarm flags, an optional indication of a state of a transmitter disable input pin, an optional indication of a state of a software disable feature of the optoelectronic transceiver, and a password that controls access to the memory (Table 3 on pages 8 and 9 discloses warning and alarm flags, Table 2 on page 8 discloses a disable state indication, and Table 1 on page 7 discloses a password).

Regarding claim 38, Stewart et al. disclose an optoelectronic transceiver (Figures 2 and 3), comprising:

a housing (page 2, paragraph [0028];

a laser transmitter 103 at least partially contained within the housing;

a photodiode receiver 102 at least partially contained within the housing;

circuitry at least partially contained, the circuitry comprising:

analog to digital conversion circuitry 127 configured to convert analog signals corresponding to operating conditions of an optoelectronic transceiver into digital values (page 3, paragraphs [0035]-[0037]);

memory (EEPROMs 120, 122, and 128) configured to store the digital values in predefined memory mapped locations identified by unique addresses, where the digital values comprise: a temperature of the optoelectronic transceiver, an internal supply voltage of the optoelectronic transceiver, a laser bias current of the laser transmitter, an

output power of the laser transmitter, and a received optical power of the photodiode receiver (page 3, paragraphs [0035]-[0037]); and

an interface 121 configured to enable a host having the addresses to read the digital values from the predefined memory mapped locations in memory (page 3, paragraphs [0029]-[0037]).

3. Claims 8-14, 17-19, 24-27, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Chieng et al. (US 6,862,302 B2)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 8, Chieng et al. disclose an integrated circuit for controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver (Figures 2 and 3), comprising:

memory (EEPROMs 120, 122, and 128) including one or more memory arrays for storing information related to the transceiver in predefined memory mapped locations of the memory the stored information including digital values corresponding to current operating conditions of the optoelectronic transceiver, where the digital values include a temperature of the optoelectronic transceiver, an internal supply voltage of the optoelectronic transceiver, a laser bias current of the

laser transmitter, an output power of the laser transmitter, and a received optical power of the photodiode receiver (column 6, lines 7-32);

analog to digital conversion circuitry 127 for receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic transceiver, converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one of the predefined memory mapped locations in the memory (column 6, lines 7-32);

control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory (column 5, lines 6-58);

an interface 121 for allowing a host to read from host specified locations within the memory, including the predefined memory mapped locations of the memory, so as to obtain one or more of the digital values corresponding to current operating conditions of the optoelectronic transceiver (column 4, lines 24-48); and

wherein the control circuitry includes circuitry configured to adjust one or more control signals in accordance with an adjustment value stored in the memory by the host via the interface (Chieng et al. disclose adjustment/"margining" values; column 4, lines 61-65).

Regarding claim 9, Chieng et al. disclose that the adjustment value corresponds to a deviation from a configured operating condition of the optoelectronic transceiver (column 4, lines 61-65).

Regarding claim 10, Chieng et al. disclose that the control circuitry is configured to adjust the one or more control signals by scaling the control signals (column 4, lines 61-65).

Regarding claim 11 Chieng et al. disclose that the control circuitry is configured to adjust the one or more control signals by an amount specified by the adjustment value (column 4, lines 61-65).

Regarding claim 12, Chieng et al. disclose a method of controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver (Figures 2 and 3), comprising:

in accordance with instructions received from a host device, enabling the host device to read from and write to host specified locations within a controller of the optoelectronic transceiver (using interface 121 and EEPROMs 120, 122, and 128), the host specified locations including a set of predefined memory mapped locations in which are stored digital values corresponding to current operating conditions of the optoelectronic transceiver, the stored digital values including a temperature of the optoelectronic transceiver, an internal supply voltage of the optoelectronic transceiver, a laser bias current of the laser transmitter, an output power of the laser transmitter, and a received optical power of the photodiode receiver (column 4, lines 24-48; column 6, lines 7-32);

receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values (using analog to digital converter 127) , and storing the digital values in the controller, the converted digital values including the digital values corresponding to current operating conditions of the optoelectronic transceiver (column 6, lines 7-32); and

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in predefined memory mapped locations within the controller (column 5, lines 6-58); and

testing operation of the device at a known deviation from a configured operating condition of the optoelectronic transceiver by adjusting one or more control signals in accordance with an adjustment value stored in the controller (column 4, lines 61-65).

Regarding claim 13, Chieng et al. disclose that the adjusting includes scaling the control signals by the adjustment value (column 4, lines 61-65).

Regarding claim 14, Chieng et al. disclose a circuit for an optoelectronic transceiver, which includes a laser transmitter and a photodiode receiver (figures 2 and 3), the circuit comprising:

analog to digital conversion circuitry 127 configured to convert analog signals corresponding to operating conditions of the optoelectronic transceiver into digital values;

memory (EEPROMs 120, 122, and 128) configured to store the digital values in predefined memory mapped locations, where the digital values stored in the predefined memory mapped locations include: a temperature of the optoelectronic transceiver, an internal supply voltage of the optoelectronic transceiver, a laser bias current of the laser transmitter, an output power of the laser transmitter, and a received optical power of the photodiode receiver (column 6, lines 7-32); and

an interface 121 configured to enable a host to read from the predefined memory mapped locations in memory (column 4, lines 24-48).

Regarding claim 17, Chieng et al. disclose a temperature sensor 125 for measuring the temperature of the optoelectronic transceiver (column 6, lines 7-15).

Regarding claim 18, Chieng et al. disclose a supply voltage sensor 126 for measuring the supply voltage of the optoelectronic transceiver (column 6, lines 24-32).

Regarding claim 19, Chieng et al. disclose that the interface is also configured to enable the host to read from and write to host-specified memory mapped addresses within the memory (column 4, lines 24-48).

Regarding claim 24, Chieng et al. disclose control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in memory (column 5, lines 6-58).

Regarding claim 25, Chieng et al. disclose that the control circuitry includes operation disable circuitry configured to disable operation of at least part of the optoelectronic transceiver (column 4, lines 14-18).

Regarding claim 26, Chieng et al. disclose that the memory further comprises one or more memory arrays for storing information related to the optoelectronic transceiver (column 4, lines 28-48).

Regarding claims 27 and 29, Chieng et al. disclose that a portion of the memory is reserved for optional warning/alarm flags (column 6, lines 16-23).

Allowable Subject Matter

4. Claims 1-7 are allowed.

5. Claims 21 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicants' arguments, see pages 10-14, filed 13 March 2006, with respect to claims 1-7, 21, and 22 have been fully considered and are persuasive in view of the accompanying

amendments to the claims. Claims 1-7, 21, and 22 are allowed or would be allowable if rewritten in independent form as noted above under "Allowable Subject Matter."

7. Applicants' arguments with respect to claims 8-20 and 23-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 6:30 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christina Y Leung
CHRISTINA LEUNG
PRIMARY EXAMINER